# TONY LAUNDRIE

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## SUMMARY


**Senior Electrical and Computer Engineer** with extensive knowledge of digital electronics development including physical design, logic design, design verification, and circuit design. Efficient CAD tool programmer, using advanced algorithms and clever tricks to manipulate text-based and graphical data. Record of improving project schedules through efficient design entry, design reuse, CAD flow development, and clear documentation.


## TECHNICAL SKILLS

Custom VLSI design and layout (standard cells, I/O, memory, clocking), ASIC logic design, logic synthesis, hierarchical floorplanning, place and route, simulation, verification, hardware debugging, Verilog, VHDL, Synopsys, Magma, Cadence, Encounter, DRC, LVS, Hspice, IBM Tools (Chipbench, Chipedit, Einstimer). Worked in CMOS process nodes: 7nm, 22nm, 32nm, 45nm, 65nm, 90nm, 180nm. Programming Languages: Perl, TCL, Cadence SKILL, C, C++, Assembly, sh/csh, HTML, PHP, X windows, Win32::GUI. Electronics hobbyist.

## EMPLOYMENT

**GlobalFoundries**, Malta, NY **Jun 2016 – Present**

**Test Chip Design/Measurement/Automation Engineer**

Wrote Cadence Skill code to automate standard cell layout in 7nm sea-of-wires finfet technology, driven by a spreadsheet to tweak numerous process parameters and DRC rules. Wrote Skill and perl code for parameterized cells of CML buffer stages and ring oscillators, again driven by spreadsheets to adjust many width/spacing/configuration values and eventually measure test chips to determine maximum performance and robust reliability.

**Rohde & Schwarz**, Beaverton, OR **Apr 2013 – Mar 2016**

**Physical Design Engineer**

Physical design for large digital signal processing blocks within complex analog signal generation and measurement chips. In addition to mixed-signal PD tasks (floorplanning, time budgeting, place-and-route, timing checks, SI checks, DRC/LVS), I also programmed unique automatic routing solutions for tight balanced differential-pair wiring and segmented regulated power supply distribution within the Cadence Encounter & Virtuoso environments, resulting in compact designs and extremely low-noise, high-quality Rohde & Schwarz products. Leading other physical design engineers in US and Germany through methodology development and education.

**Vitesse/SigNet**, Austin, TX (telecommuter/contract) **May 2012 – Dec 2012**

**Physical Design Engineer**

Responsible for physical design and timing/DRC closure for several large blocks containing memory macros in a digital ASIC using Magma software. Quickly learned tool flow and wrote scripts as needed to simplify and document processing steps.

**IBM**, Rochester, MN (telecommuter) **2005 – 2012**

**Senior Physical Design Engineer & CAD Programmer**

Improved productivity for a team of 15 physical design and CAD tool engineers working primarily on processor chips for the Xbox, Wii, and Playstation, as well as large custom chips for IBM servers. Performed a variety of physical design tasks: floorplanning, port assignment, balanced/shielded wiring, signal buffering, placement of test/scan logic, bitstacking, data translation, and DRC/LVS verification in IC technologies down to 22nm.

- Assisted with low-skew clock mesh design and layout, through early spreadsheet estimation, computerized drawing, sketch-driven simulation, and optimization of buffer sizes and wire widths.
- Wrote thousands of lines in Perl, TCL, and Cadence SKILL to eliminate tedious tasks.
- Wrote visualization tools and hotkey-triggered functions to simplify manual processes.
- Made small team of 10 work-at-home employees more productive and better connected through gatherings and regular email communication.

**CRAY / SILICON GRAPHICS**, Chippewa Falls, WI **1993 – 2005**

**Senior Physical Design Engineer, Circuit Designer, Logic Designer, CAD Programmer**

Performed wide variety of engineering tasks through multiple supercomputer projects.

- Floorplanned, placed, and routed large system chips containing multiple clock domains and voltages, asynchronous paths, voltage islands, and many memory blocks.
- Wrote Perl, TCL, and SKILL scripts to simplify repetitive tasks.
- Wrote other code to work around bugs in commercial programs.
- Drew and verified layouts for custom I/O and standard cells.
- Performed Cadence technology file setup, coded parameterized cells, and created many custom menu functions in Virtuoso.
- Presented papers at the International Cadence Usergroup conference: laundrie.org/cadence
- Created circuits and layouts for BiCMOS custom memory blocks.
- Helped create BiCMOS standard cell library, automating the entire process from layout, DRC and LVS, parasitic extraction, Spice simulation, and timing model creation.

## PREVIOUS EXPERIENCE

**ASIC Logic Design Verification Engineer**

Wrote Verilog and performed gate-level simulation of computer ASICs.

**Board-Level Logic Design Engineer**

Designed video processing boards for military airplanes.

## EDUCATION

- **MS**, Electrical and Computer Engineering, University of Wisconsin, Madison, WI
  - Studied design automation, logic synthesis, fault tolerance, and VLSI design. Co-authored articles in IEEE Computer magazine on the Scalable Coherent Interface. Studied computer architecture, circuit theory, performance simulation, computer networks, and digital signal processing.
- **BS**, Electrical and Computer Engineering, University of Wisconsin, Madison, WI
  - Focused on computer science, CAD programming, and digital logic design. GPA 3.8 / 4.0, top 9% of all ECE graduates (33 / 381). Transcript available upon request.