TONY LAUNDRIE

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IC DESIGN ENGINEER

Creative Senior Electrical and Computer Engineer skilled in **ASIC RTL-to-GDS Physical Design, Layout of Standard Cells, Custom I/O, and Memory**, and **CAD Tool Programming** for building and checking complex IC structures or improving design flow efficiency.

Floorplanning | Place & Route | Static Timing Closure | Physical Verification DRC LVS Antenna
Standard Cells | Memory | I/O Cells | Clocking | SoC Top Level & Hierarchical Block Integration
Custom Layout | Layout Automation at Transistor & Chip Levels | ASIC CAD Flows
Circuit Design & Simulation | Logic Design & Synthesis | DFT | Logic Design Verification

Design Entry:	Verilog, VHDL, Spice, Hspice, Cadence Schematics
Design Tools:	**Cadence**: Virtuoso, Innovus Encounter, Tempus STA, Pcells, Conformal **Synopsys**: ICC, DC, PrimeTime STA **Other**: Calibre DRC LVS, KLayout, IBM ChipBench ChipEdit
Process Nodes:	IBM, TSMC, GlobalFoundries down to 7nm
Programming Languages:	Perl, TCL, Cadence Skill Pcells, C, C++, Assembly, Python, csh, PHP, HTML, Linux, Windows, X, Win::GUI

EMPLOYMENT

GlobalFoundries, Malta, NY **2016 – 2018**
Physical Design Engineer (remote)

- Standard Cell and Custom Block Layout & Layout Automation for 7nm Process Node.
- Automatically built cutting-edge 7nm sea-of-wires finfet standard cells, ring oscillators, and transistor experiments utilizing mixture of Skill code, parameterized cells, spreadsheets, and other supporting code.
- Automated DRC, LVS, and Spice model generation.
- Recognized as the go-to programmer within the group for miscellaneous tasks like Synopsys timing library generation and analysis, automated shape processing, and DRC fixup, mentoring users of such code to enable them to make individual improvements.

Rohde & Schwarz, Beaverton, OR **2013 – 2016**
Physical Design Engineer

- Floorplanning, Place-and-route, Timing & DRC Closure for Large Signal Processors.
- Invented novel automatic floor planning and routing methods for low-noise segmented regulated power supply distribution and tightly-balanced differential-pair wiring.
- Set up technology files for Cadence Encounter floorplanning, place-and-route, and physical design checks in mixed-signal environment, responsible for back-end physical verification.

Vitesse / SigNet, Austin, TX **2012**
Physical Design Engineer (remote, 6-month contract)

- Synthesis, Place-and-route, Timing & DRC Closure of several blocks using Magma Tools.

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IBM, Rochester, MN **2005 – 2012**
Physical Design Engineer (mostly remote)

- Floorplanning, Place-and-route, Clock Wiring, Timing & DRC Closure, Game & Server ASICs.
- Built low-skew clock meshes in Xbox, Wii, PlayStation, and IBM processors, through early spreadsheet estimation, computerized drawing, sketch-driven simulation, and size optimization of buffers and clock wires.
- Wrote repeatable, reusable, and well-organized code for top-level floorplanning, placement, routing, global signal buffering, test scan logic insertion, noise and timing analysis, and DRC cleanup.
- Enriched team morale and productivity of small team of work-at-home employees through educational or social gatherings and regular online communication.

CRAY / SILICON GRAPHICS, Chippewa Falls, WI
Physical Design Engineer
Standard Cell, Memory, and custom SerDes blocks circuit and logic design, plus CAD development.

Supercomputer Systems, Eau Claire, WI
Logic Design Engineer, DV
Memory system design and simulation. ASIC Logic Design Verification.

Astronautics Corporation, Milwaukee, WI
Electrical Engineer
Military Video System Logic Design, from initial specification to final circuit boards.

EDUCATION

Master of Science (MS), Electrical & Computer Engineering, University of Wisconsin, Madison, WI

- Focused on design automation, logic synthesis, DFT/fault tolerance, VLSI, computer architecture.
- Co-authored articles in IEEE Computer magazine on the Scalable Coherent Interface.

Bachelor of Science (BS), Electrical & Computer Engineering, University of Wisconsin, Madison, WI

- Focused on computer science, networking, CAD programming, digital logic design.
- GPA 3.8 / 4.0, top 9% of all ECE graduates (33 / 381).

Community Theatre Actor, Singer, Carpenter, Sound/Lighting Tech | Videographer | Eagle Boy Scout